I CLAIM

1. A method for creating and testing a channel decoder with built-in self-test comprising:

simulating the channel decoder architecture and operation;

modifying the simulated channel decoder for built-in self-test;

creating a production test signal as a product of the modified channel decoder simulation;

manufacturing a channel decoder patterned after the modified channel decoder simulation; and

testing the manufactured channel decoder using the production test signal.

2. The method for claim 1 wherein the production test signal tests a combination of analog and digital circuits of the channel decoder.

3. The method for claim 1 wherein the production test signal tests a digital circuit of the channel decoder.

4. The method for built-in self-test of a channel decoder of claim 1 further comprising collecting a result of the manufactured channel decoder under test using low-end test equipment.

5. The method for claim 4 wherein a transient time interval is performed prior to collecting the result.

6. The method for claim 4 wherein the result is a number of collected errors.

7. The method for claim 4 wherein the result is a signature difference.

8. The method for claim 4 wherein the result is collected by an error correction unit.

9. A method for modifying a channel decoder for built-in self-test comprising:
identifying memory resources of the channel decoder;
creating a periodic test signal from a provided test message; and
modifying the channel decoder dependent on the memory resources and the periodic test signal.

10. The method for modifying a channel decoder of claim 9 further comprising modifying the channel decoders communication standard.

11. The method for modifying a channel decoder of claim 9 wherein the memory resources are located in a digital demodulator.

12. The method for modifying a channel decoder of claim 9 wherein the memory resources are located in a RAM-containing block.

13. The method for modifying a channel decoder of claim 9 wherein the memory resources are located in a RAM module.

14. The method for modifying a channel decoder of claim 9 wherein the memory resources are located in a ROM module.

15. The method for modifying a channel decoder of claim 9 wherein the test message is composed of random symbols.

16. A method for producing a production test signal for a built-in self-test channel decoder comprising:

creating a test message;

modulating the test message;

encoding the modulated test message;

selecting a subset of the encoded, modulated test message;

creating the production test signal based on the selected sequence; and

storing the production test signal on a storage device.

17. The method for producing a production test signal of claim 16 further comprising integrating channel impairments to the modulated digital test signal.

18. The method for producing a production test signal of claim 16 wherein a test message size denoted *s* and expressed in symbols, is made short enough that a number of samples denoted b, will be smaller than available memory capacity using the relation between the two values $b = s \times \frac{fc}{fs}$, where fc is a sampling (clock) frequency and fs is the symbol frequency.

19. The method for producing a production test signal of claim 16 wherein the digital test signal is modulated using a delta-sigma modulator.

20. A method for testing a built-in self-test channel decoder comprising:

initializing internal memory of the channel decoder;

downloading a production test signal to the internal memory;

producing a periodic test signal as a timed replication of the production test signal; and

supplying the periodic test signal to a circuit under test.

21. The method for testing of claim 20 further comprising changing the periodic test signal from digital to analog.

22. The method for testing of claim 20 further comprising integrating signal impairments to the periodic test signal.

23. The method for testing of claim 20 wherein the internal memory is omitted from testing.

24. The method for testing of claim 20 further comprising setting at least one stimulus injection switch to a condition dependent of the channel decoder circuit being tested.

25. The method for testing of claim 20 further comprising reducing a high frequency content of the periodic analog test signal using a first-order RC low pass filter.

26. The method for testing of claim 20 wherein the circuit under test is a combination of analog and digital circuits.

27. The method for testing of claim 20 wherein the circuit under test is digital.

28. A channel decoder made by the process comprising the steps of:

identifying memory resources of the channel decoder;

creating a periodic test signal from a provided test message;

modifying a channel decoder communication standard dependent on the memory resources and the periodic test signal; and

modifying the channel decoder to incorporate the modified communication standard and predefined circuitry.

29. A channel decoder comprising:

a radio frequency circuit;

a intermediate frequency circuit in communication with the radio frequency circuit;

a analog to digital converter in communication with the intermediate frequency circuit;

a digital demodulator in communication with the analog to digital converter wherein the digital demodulator allows for modification of the channel decoders communication standard;

a switch in communication with the digital demodulator and the intermediate frequency circuit; and

a signal generation circuit in communication with the digital demodulator.

30. The channel decoder of claim 29 wherein the switch is in communication with the digital demodulator and the analog to digital converter.

31. The channel decoder of claim 29 wherein the signal generation circuit comprises:

a address generator;

a memory bank in communication with the address generator; and

a serializer in communication with the memory bank.

32. The channel decoder of claim 31 further comprising a digital to analog converter in communication with the serializer.

33. The channel decoder of claim 32 wherein the digital to analog converter is a one bit digital to analog converter.

34. A apparatus for modifying a channel decoder for built-in self-test comprising:

means for identifying memory resources of the channel decoder;

means for creating a periodic test signal from a provided test message; and

means for modifying the channel decoder dependent on the memory resources and the periodic test signal.

35. A apparatus for producing a production test signal for a built-in self-test channel decoder comprising:

means for creating a test message;

means for modulating the test message;

means for encoding the modulated test message;

means for selecting a subset of the encoded, modulated test message;

means for creating the production test signal based on the selected sequence; and

means for storing the production test signal on a storage device.

36. A apparatus for testing a built-in self-test channel decoder comprising:

means for initializing internal memory of the channel decoder;

means for downloading a production test signal to the internal memory;

means for producing a periodic test signal as a timed replication of the production test signal; and

means for supplying the periodic test signal to a circuit under test.

37. A computer readable medium including a computer program for modifying a channel decoder for built-in self-test comprising:

computer readable code for identifying memory resources of the channel decoder;

computer readable code for creating a periodic test signal from a test message; and

computer readable code for modifying the channel decoder dependent on the memory resources and the digital test signal.

38. A computer readable medium including a computer program for producing a production test signal for a built-in self-test channel decoder comprising:

computer readable code for creating a test message;

computer readable code for modulating the test message;

computer readable code for encoding the modulated test message;

computer readable code for selecting a subset of the encoded, modulated test message;

computer readable code for creating the production test signal based on the selected sequence; and

computer readable code for storing the production test signal on a storage device.

39. A computer readable medium including a computer program for testing a built-in self-test channel decoder comprising:

computer readable code for initializing internal memory of the channel decoder;

computer readable code for downloading a production test signal to the internal memory;

computer readable code for producing a periodic test signal as a timed replication of the production test signal; and

computer readable code for supplying the periodic test signal to a circuit under test.